AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions or listings of claims for this application.

Listing of Claims:

Claims 1-14 (Canceled).

15. (Previously presented) A method of forming a pixel, comprising:

forming a photosensor on a substrate, said photosensor detecting and storing photon energy;

forming a transfer transistor having a gate on said substrate and adjacent said photosensor;

forming a reset transistor having a gate on said substrate and on a side of said transfer transistor gate opposite said photosensor;

forming a floating diffusion region on said substrate and between said transfer and reset transistor gates; and

forming a gate capacitor over said substrate, the gate capacitor being located between said transfer and reset transistor gates and electrically connected to the floating diffusion region.

16. (Previously presented) The method of claim 15, wherein the gate capacitor is formed over a portion of said floating diffusion region and an active area of said substrate.

17. (Previously presented) A pixel of an imager, said pixel comprising:

a photosensing region which receives incident light and generates photoelectric charges;

a transfer transistor having a gate on said substrate and adjacent said photosensor;

a reset transistor having a gate on said substrate and on a side of said transfer transistor gate opposite said photosensor;

a diffusion region for receiving photogenerated charges from said photosensing region, said diffusion region being between said transfer and reset transistor gates; and

at least one capacitor switchably operable to increase capacitance of said diffusion region, said capacitor having a gate located between said transfer and reset transistor gates.

Claims 18-26 (Canceled).

27. (Original) A CCD imager system, comprising:

a processor; and

a CCD imager coupled to said processor, said CCD imager comprising:

a register for inputting and outputting photo-generated charge;

a storage node, connected to receive the photo-generated charge from said register; and

at least one gate capacitor connected to the storage node, each gate capacitor being selectively operable to increase a charge storage capacitance of the storage node.

28. (Previously presented) The system of claim 27, further comprising timing and control circuitry for generating a timing signal to selectively operate the at least one gate capacitor.

29. (Previously presented) The method of claim 15, wherein gates of said reset transistor, transfer transistor and gate capacitor are formed at a same processing step.

30. (Previously presented) The method of claim 15, wherein the gate capacitor is formed over a portion of an isolation region.